DATA SHEET

TJA1020
LIN transceiver

Product specification
Supersedes data of 2001 Dec 17

2002 Jul 17

FEATURES

General

- Baud rate up to 20 Kbaud
- Very low ElectroMagnetic Emission (EME)
- High ElectroMagnetic Immunity (EMI)
- Low slope mode for an even further reduction of EME
- Passive behaviour in unpowered state
- Input levels compatible with 3.3 and 5 V devices
- Integrated termination resistor for Local Interconnect Network (LIN) slave applications
- Wake-up source recognition (local or remote).

Low power management

- Very low current consumption in sleep mode with local and remote wake-up.

Protections

- Transmit data (TXD) dominant time-out function
- Bus terminal and battery pin protected against transients in the automotive environment (ISO7637)
- Bus terminal short-circuit proof to battery and ground
- Thermally protected.

GENERAL DESCRIPTION

The TJA1020 is the interface between the LIN master/slave protocol controller and the physical bus in a Local Interconnect Network (LIN). It is primarily intended for in-vehicle sub-networks using baud rates from 2.4 up to 20 Kbaud.

The transmit data stream of the protocol controller at the TXD input is converted by the LIN transceiver into a bus signal with controlled slew rate and wave shaping to minimize EME. The LIN bus output pin is pulled HIGH via an internal termination resistor. For a master application an external resistor in series with a diode should be connected between pin INH or pin BAT and pin LIN. The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller.

In normal transceiver operation the TJA1020 can be switched in the normal slope mode or the low slope mode. In the low slope mode the TJA1020 lengthens the rise and fall slopes of the LIN bus signal, thus further reducing the already very low emission in normal slope mode.

In sleep mode the power consumption of the TJA1020 is very low, whereas in failure modes the power consumption is reduced to a minimum.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{BAT}	supply voltage on pin BAT	5	12	27	V
I_{BAT}	supply current on pin BAT in sleep mode	1	3	8	µA
	supply current on pin BAT in standby mode; bus recessive	100	400	1000	µA
	supply current on pin BAT in normal slope mode; bus recessive	100	400	1000	µA
	supply current on pin BAT in normal slope mode; bus dominant	1	3.5	8.0	mA
V_{LIN}	DC voltage on pin LIN	–27	–	+40	V
T_{vj}	virtual junction temperature	–40	–	+150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage; human body model; pins NWAKE, LIN and BAT	–4	–	+4	kV

ORDERING INFORMATION

TYPE NUMBER	PACKAGES		
	NAME	DESCRIPTION	VERSION
TJA1020T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1020U	–	bare die; die dimensions 1480 × 1760 × 375 µm	–

BLOCK DIAGRAM

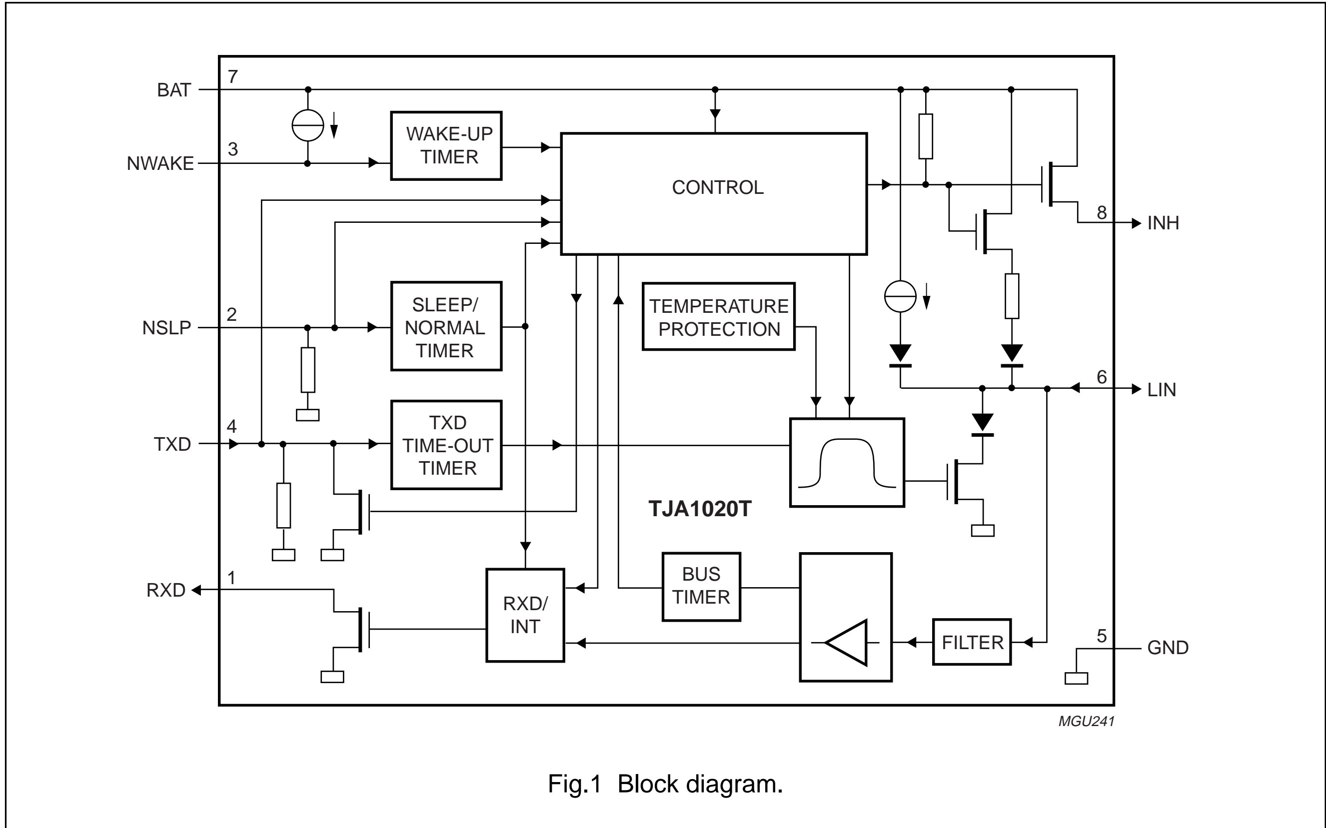


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RXD	1	receive data output (open-drain); active LOW after a wake-up event
NSLP	2	sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD
NWAKE	3	local wake-up input (active LOW); negative edge triggered
TXD	4	transmit data input; active LOW output after a local wake-up event
GND	5	ground
LIN	6	LIN bus line input/output
BAT	7	battery supply
INH	8	battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event

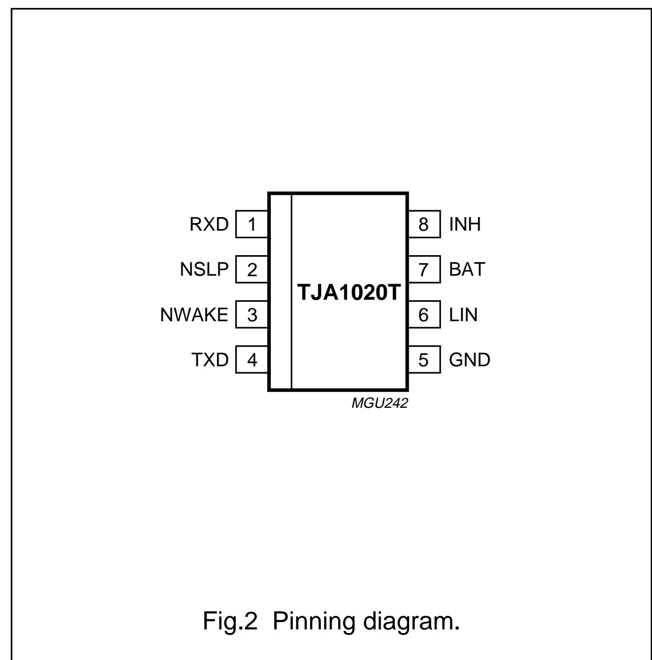


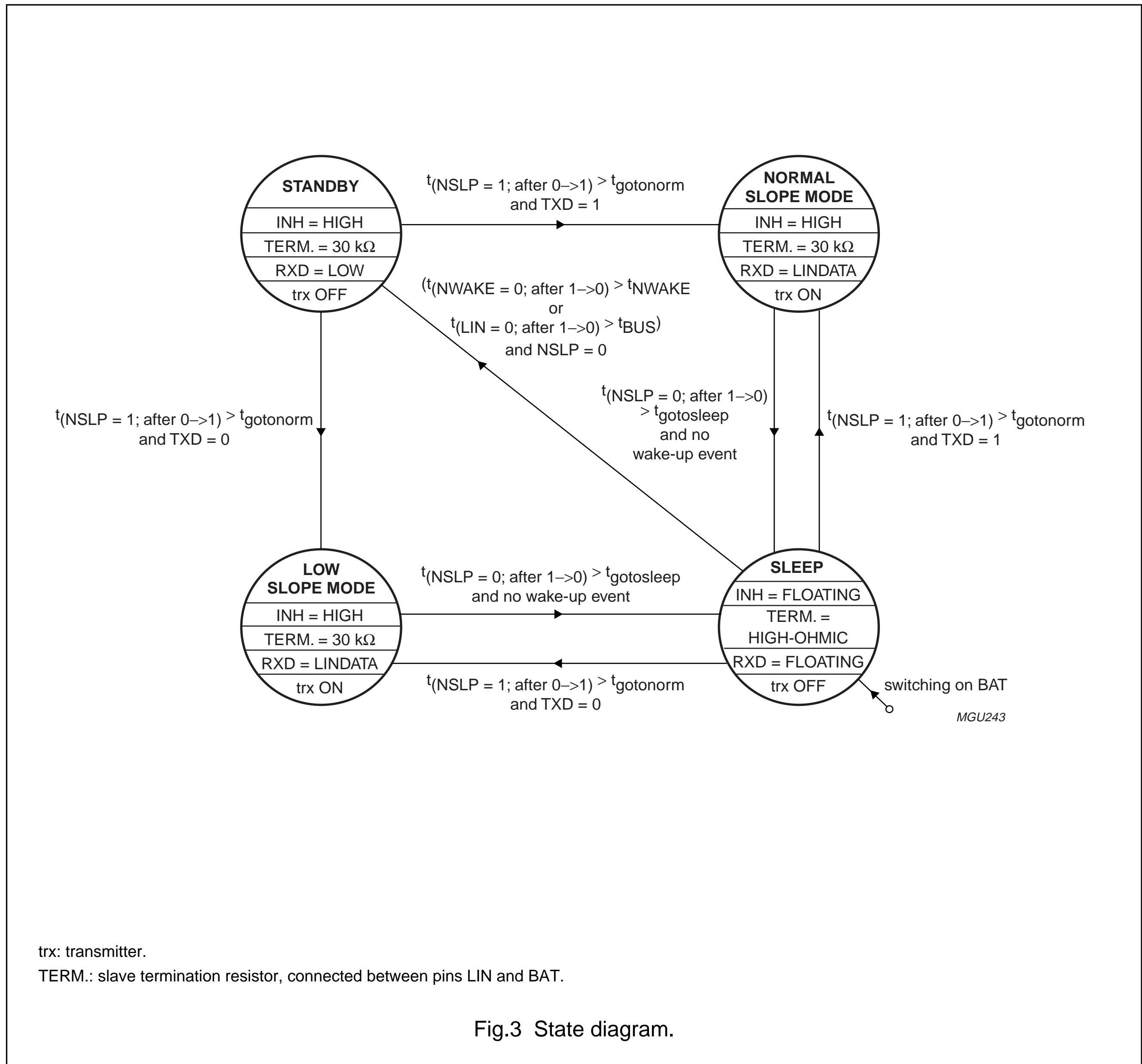
Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TJA1020 is the interface between the LIN master/slave protocol controller and the physical bus in a Local Interconnect Network (LIN). The LIN transceiver is optimized for the maximum specified LIN transmission speed of 20 Kbaud providing optimum EMC performance due to wave shaping of the LIN output.

Operating modes

The TJA1020 provides two modes of normal operation, one intermediate mode and one very low power mode. Figure 3 shows the state diagram.



trx: transmitter.

TERM.: slave termination resistor, connected between pins LIN and BAT.

Fig.3 State diagram.

Table 1 Operating modes

MODE	NSLP	TXD (OUTPUT)	RXD	INH	TRANSMITTER	REMARKS
Sleep	0	weak pull-down	floating	floating	off	no wake-up request detected
Standby[1]	0	weak pull-down if remote wake-up; strong pull-down if local wake-up; note 2	LOW; note 3	HIGH	off	wake-up request detected; in this mode the microcontroller can read the wake-up source: remote or local wake-up
Normal slope mode	1	weak pull-down	HIGH: recessive state LOW: dominant state	HIGH	normal slope mode	notes 2, 3 and 4
Low slope mode	1	weak pull-down	HIGH: recessive state LOW: dominant state	HIGH	low slope mode	notes 2, 3 and 5

Notes

1. The standby mode is entered automatically upon any local or remote wake-up event during sleep mode. Pin INH and the 30 kΩ termination resistor at pin LIN are switched on.
2. The internal wake-up source flag (set if a local wake-up did occur and fed to pin TXD) will be reset when entering normal slope or low slope mode (NSLP goes HIGH).
3. The wake-up interrupt (on pin RXD) is released when entering normal slope or low slope mode (NSLP goes HIGH).
4. The normal slope mode is entered if TXD is set HIGH (set by the microcontroller to recessive) during a positive edge on NSLP. In the event of a short-circuit to ground on pin TXD, the transmitter will be disabled.
5. The low slope mode is entered if pin TXD is pulled LOW (actively set dominant by the microcontroller or due to a failure on TXD) during the positive edge on NSLP.

Sleep mode

This mode is the most power saving mode of the TJA1020 and the default state after power-up (first battery supply). Despite its extreme low current consumption, the TJA1020 can still be waken up remotely via pin LIN, or waken up locally via pin NWAKE, or activated directly via pin NSLP. Filters at the inputs of the receiver (LIN), of pin NWAKE and of pin NSLP are preventing unwanted wake-up events due to automotive transients or EMI. All wake-up events have to be maintained for a certain time period (t_{BUS}, t_{NWAKE} and $t_{gotonorm}$).

The sleep mode is initiated by a falling edge on the pin NSLP driven by the microcontroller. After a filter time continuously driven sleep command (pin NSLP = LOW), pin INH becomes floating.

In sleep mode the internal slave termination between pins LIN and BAT is disabled to minimize the power dissipation in case pin LIN is short-circuited to ground. Only a weak pull-up between pins LIN and BAT is present.

The sleep mode can be activated independently from the actual level on pin LIN or NWAKE. So it is guaranteed that the lowest power consumption is achievable even in case of a continuous dominant level on pin LIN or a continuous LOW on pin NWAKE.

Standby mode

The standby mode is entered automatically whenever a local or remote wake-up occurs while the TJA1020 is in its sleep mode. These wake-up events activate pin INH and enable the slave termination resistor at the pin LIN. As a result of the HIGH condition on pin INH the voltage regulator and the microcontroller can be activated.

The standby mode is signalled by a LOW level on pin RXD which can be used as an interrupt for the microcontroller.

In the standby mode (pin NSLP is still LOW), the condition of pin TXD (weak pull-down or strong pull-down) indicates the wake-up source: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request.

Setting pin NSLP HIGH during standby mode results in the following events:

- An immediate reset of the wake-up source flag; thus releasing the possible strong pull-down at pin TXD before the actual mode change (after $t_{gotonorm}$) is performed
- A change into normal slope mode if the HIGH level on pin NSLP has been maintained for a certain time period ($t_{gotonorm}$) and pin TXD is HIGH
- A change into low slope mode if the HIGH level on pin NSLP has been maintained for a certain time period ($t_{gotonorm}$) and pin TXD is pulled LOW by the application. In the event of a short-circuit to ground or an open-wire on pin TXD, the LIN output remains recessive (fail safe).
- A reset of the wake-up request signal on pin RXD if the HIGH level on pin NSLP has been maintained for a certain time period ($t_{gotonorm}$).

Normal slope mode

In the normal slope mode the transceiver is able to transmit and receive data via the LIN bus line. The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller (see Fig.1): HIGH at a recessive level and LOW at a dominant level on the bus. The receiver has a supply voltage related threshold with hysteresis and an integrated filter to suppress bus line noise. The transmit data stream of the protocol controller at the TXD input is converted by the transmitter into a bus signal with controlled slew rate and wave shaping to minimize EME. The LIN bus output pin is pulled HIGH via an internal slave termination resistor. For a master application an external resistor in series with a diode should be connected between pin INH or BAT on one side and pin LIN on the other side.

The normal slope mode is entered by a HIGH level on pin TXD and a HIGH level on pin NSLP maintained for a certain time period ($t_{gotonorm}$), coming from the sleep or standby mode.

The TJA1020 switches to sleep mode in case of a LOW level on pin NSLP, maintained during a certain time period ($t_{gotosleep}$).

Low slope mode

The only difference between the normal slope mode and the low slope mode is the transmitter behaviour.

In the low slope mode the transmitter output stage drives the LIN bus line with lengthened rise and fall slopes. This will further reduce the already outstanding EME in the normal slope mode. The low slope mode is perfectly suited for applications where transmission speed is not critical. The mode selection is done by the LIN transceiver after a positive edge on pin NSLP, maintained for a certain time period ($t_{gotonorm}$). If pin TXD is LOW at that time, the low slope mode is entered, otherwise the normal mode is entered. The transition to the low slope mode will be executed during an open pin TXD (fail-safe), a short-circuit from pin TXD to ground (fail-safe) or an intended LOW level of pin TXD programmed by the microcontroller. The transmitter is enabled after a LOW-to-HIGH transition on pin TXD. In the event of a short-circuit to ground on pin TXD, the transmitter will be disabled.

Wake-up

There are three ways to wake-up a TJA1020 which is in sleep mode:

1. Remote wake-up via a dominant bus state
2. Local wake-up via a negative edge at pin NWAKE
3. Mode change (pin NSLP is HIGH) from sleep mode to normal slope/low slope mode.

Remote and local wake-up

A falling edge at pin NWAKE followed by a LOW level maintained for a certain time period (t_{NWAKE}) results in a local wake-up. The pin NWAKE provides an internal pull-up towards pin BAT.

If, during power-up, pin NWAKE is LOW for a certain period of time (t_{NWAKE}) this will also result in a local wake-up.

A falling edge at pin LIN followed by a LOW level maintained for a certain time period (t_{BUS}) and a rising edge at pin LIN respectively (see Fig.4) results in a remote wake-up.

After a local or remote wake-up pin INH is activated (it goes HIGH) and the internal slave termination resistor is switched on. The wake-up request is indicated by a LOW active wake-up request signal on pin RXD to interrupt the microcontroller.

Wake-up via mode transition

It is also possible to set pin INH HIGH with a mode transition towards normal slope/low slope mode via pin NSLP. This is useful for applications with a continuously powered microcontroller.

Wake-up source recognition

The TJA1020 can distinguish between a local wake-up request on pin NWAKE and a remote wake-up request via a dominant bus state. The wake-up source flag is set in case the wake-up request was a local one. The wake-up source can be read on pin TXD in the standby mode. If an external pull-up resistor on pin TXD to the power supply voltage of the microcontroller has been added a HIGH level indicates a remote wake-up request (weak pull-down at pin TXD) and a LOW level indicates a local wake-up request (strong pull-down at pin TXD; much stronger than the external pull-up resistor).

The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately, if the microcontroller sets pin NSLP HIGH.

TXD dominant time-out function

A ‘TXD Dominant Time-out’ timer circuit prevents the bus line from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

Fail-safe features

Pin TXD provides a pull-down to GND in order to force a predefined level on input pin TXD in case the pin TXD is unsupplied.

Pin NSLP provides a pull-down to GND in order to force the transceiver into sleep mode in case the pin NSLP is unsupplied.

Pin RXD is set floating in case of lost power supply on pin BAT.

The current of the transmitter output stage is limited in order to protect the transmitter against short-circuit to pins BAT or GND.

A loss of power (pins BAT and GND) has no impact to the bus line and the microcontroller. There are no reverse currents from the bus. The LIN transceiver can be disconnected from the power supply without influencing the LIN bus.

The output driver at pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the thermal protection circuit disables the output driver. The driver is enabled again if the junction temperature has been decreased below $T_{j(sd)}$ and a recessive level is present at pin TXD.

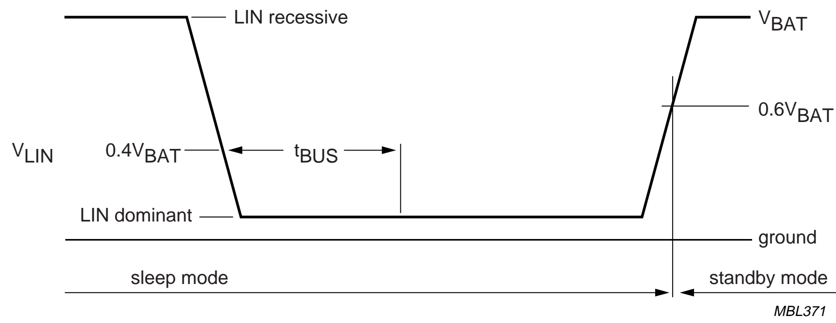


Fig.4 Wake-up behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BAT}	supply voltage on pin BAT		–0.3	+40	V
V_{TXD}, V_{RXD}, V_{NSLP}	DC voltage on pins TXD, RXD and NSLP		–0.3	+7	V
V_{LIN}	DC voltage on pin LIN		–27	+40	V
V_{NWAKE}	DC voltage on pin NWAKE		–1	+40	V
I_{NWAKE}	current on pin NWAKE (only relevant if $V_{NWAKE} < V_{GND} – 0.3$ V; current will flow into pin GND)		–15	–	mA
V_{INH}	DC voltage on pin INH		–0.3	V_{BAT} + 0.3	V
I_{INH}	output current at pin INH		–50	+15	mA
$V_{trt(LIN)}$	transient voltage on pin LIN (ISO7637)		–150	+100	V
T_{vj}	virtual junction temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage; human body model	note 1			
	on pins NWAKE, LIN and BAT		–4	+4	kV
	on pins RXD, NSLP, TXD and INH		–2	+2	kV
$V_{esd(MM)}$	electrostatic discharge voltage; machine model; all pins	note 2	–200	+200	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 µH coil. In the event of a discharge from pin INH to pin BAT: $–150\ V < V_{esd(MM)} < +150\ V$.

THERMAL CHARACTERISTICS

According to IEC747-1.

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in SO8 package	in free air	145	K/W
$R_{th(j-s)}$base	thermal resistance from junction to substrate bare die	in free air	tbf	K/W

QUALITY SPECIFICATION

Quality specification in accordance with *“AEC - Q100”*.

CHARACTERISTICS

V_{BAT} = 5 to 27 V; T_{vj} = –40 to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified; notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{BAT}	supply current on pin BAT	sleep mode (V_{LIN} = V_{BAT}; V_{NWAKE} = V_{BAT}; V_{TXD} = 0 V; V_{NSLP} = 0 V)	1	3	8	μA
		standby mode; bus recessive (V_{INH} = V_{BAT}; V_{LIN} = V_{BAT}; V_{NWAKE} = V_{BAT}; V_{TXD} = 0 V; V_{NSLP} = 0 V)	100	400	1000	μA
		standby mode; bus dominant (V_{BAT} = 12 V; V_{INH} = 12 V; V_{LIN} = 0 V; V_{NWAKE} = 12 V; V_{TXD} = 0 V; V_{NSLP} = 0 V); note 3	300	900	2000	μA
		low slope mode; bus recessive (V_{INH} = V_{BAT}; V_{LIN} = V_{BAT}; V_{NWAKE} = V_{BAT}; V_{TXD} = 5 V; V_{NSLP} = 5 V)	100	400	1000	μA
		normal slope mode; bus recessive (V_{INH} = V_{BAT}; V_{LIN} = V_{BAT}; V_{NWAKE} = V_{BAT}; V_{TXD} = 5 V; V_{NSLP} = 5 V)	100	400	1000	μA
		low slope mode; bus dominant (V_{BAT} = 12 V; V_{INH} = 12 V; V_{NWAKE} = 12 V; V_{TXD} = 0 V; V_{NSLP} = 5 V); note 3	1	3.5	8	mA
		normal slope mode; bus dominant (V_{BAT} = 12 V; V_{INH} = 12 V; V_{NWAKE} = 12 V; V_{TXD} = 0 V; V_{NSLP} = 5 V); note 3	1	3.5	8	mA
Pin TXD						
V_{IH}	HIGH-level input voltage		2	–	7	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{hys}	TXD hysteresis voltage		0.03	–	0.5	V
R_{TXD}	TXD pull-down resistor	V_{TXD} = 5 V	125	350	800	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	LOW-level input current	V_{TXD} = 0 V	–5	0	+5	μA
I_{OL}	LOW-level output current (local wake-up request)	standby mode; V_{NWAKE} = 0 V; V_{LIN} = V_{BAT}; V_{TXD} = 0.4 V	1.5	3	–	mA
Pin NSLP						
V_{IH}	HIGH-level input voltage		2	–	7	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{hys}	NSLP hysteresis voltage		0.03	–	0.5	V
R_{NSLP}	NSLP pull-down resistor	V_{NSLP} = 5 V	125	350	800	kΩ
I_{IL}	LOW-level input current	V_{NSLP} = 0 V	–5	0	+5	μA
Pin RXD (open-drain)						
I_{OL}	LOW-level output current	normal slope mode; V_{LIN} = 0 V; V_{RXD} = 0.4 V	1.3	3.5	–	mA
I_{LH}	HIGH-level leakage current	normal slope mode; V_{LIN} = V_{BAT}; V_{RXD} = 5 V	–5	0	+5	μA
Pin NWAKE						
V_{IH}	HIGH-level input voltage		V_{BAT} – 1	–	V_{BAT} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	V_{BAT} – 3.3	V
I_{IL}	NWAKE pull-up current	V_{NWAKE} = 0 V	–30	–10	–3	μA
I_{LH}	HIGH-level leakage current	V_{NWAKE} = 27 V; V_{BAT} = 27 V	–5	0	+5	μA
Pin INH						
$R_{sw(INH)}$	switch-on resistance between pins BAT and INH	standby; low slope or normal slope mode; I_{INH} = –15 mA; V_{BAT} = 12 V	–	30	50	Ω
I_{LH}	HIGH-level leakage current	sleep mode; V_{INH} = 27 V; V_{BAT} = 27 V	–5	0	+5	μA
Pin LIN						
$V_{o(reces)}$	LIN recessive output voltage	V_{TXD} = 5 V; I_{LIN} = 0 mA	0.9V_{BAT}	–	V_{BAT}	V
$V_{o(dom)}$	LIN dominant output voltage	V_{TXD} = 0 V; V_{BAT} = 8 to 27 V	0.6	–	0.15V_{BAT}	V
		V_{TXD} = 0 V; V_{BAT} = 7.3 V	0.6	–	1.2	V
I_{LH}	HIGH-level leakage current	V_{LIN} = V_{BAT}	–1	0	+1	μA
I_{IL}	LIN pull-up current	sleep mode; V_{LIN} = 0 V; V_{NSLP} = 0 V	–2	–5	–10	μA
R_{SLAVE}	slave termination resistance to pin BAT	standby, low slope or normal slope mode; V_{LIN} = 0 V; V_{BAT} = 12 V	20	30	47	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(sc)}$	short-circuit output current	$V_{LIN} = V_{BAT} = 12$ V; $V_{TXD} = 0$ V; $t < t_{dom}$	27	40	60	mA
		$V_{LIN} = V_{BAT} = 27$ V; $V_{TXD} = 0$ V; $t < t_{dom}$	60	90	125	mA
$V_{th(rx)}$	receiver threshold voltage	$V_{BAT} = 7.3$ to 27 V	$0.4V_{BAT}$	–	$0.6V_{BAT}$	V
$V_{cntr(rx)}$	receiver centre voltage	$V_{BAT} = 7.3$ to 27 V	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
$V_{thr(hys)}$	receiver threshold hysteresis voltage	$V_{BAT} = 7.3$ to 27 V	$0.145V_{BAT}$	$0.16V_{BAT}$	$0.175V_{BAT}$	V
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		160	175	190	°C
AC characteristics						
$\Delta t_{d(TXD\text{-}BUSon/off)}$	TXD propagation delay failure	normal slope mode; $C_L = 10$ nF; $R_L = 500\ \Omega$; (see Fig.5) $t_{PropTxDom} - t_{PropTxRec}$	–2	0	+2	µs
$\Delta t_{d(TXD\text{-}BUSon/off)}$	TXD propagation delay failure	low slope mode; $C_L = 10$ nF; $R_L = 500\ \Omega$; (see Fig.5) $t_{PropTxDom} - t_{PropTxRec}$	–5	0	+5	µs
$\Delta t_{d(BUSon/off\text{-}RXD)}$	RXD propagation delay failure	normal slope mode and low slope mode; $C_L = 0$; $R_L = \infty$; voltage on LIN externally forced; LIN slope time <500 ns; $C_{RXD} = 20$ pF; $R_{RXD} = 2.4\ k\Omega$; (see Fig.5) $t_{PropRxDom} - t_{PropRxRec}$	–2	0	+2	µs
$t_{f(slope)(dom)}$	fall time LIN (100% to 0%)	normal slope mode; $C_L = 10$ nF; $R_L = 500\ \Omega$; $V_{BAT} = 12$ V; transition from recessive to dominant; note 4; (see Fig.5)	–	16	27	µs
$t_{r(slope)(rec)}$	rise time LIN (0% to 100%)	normal slope mode; $C_L = 10$ nF; $R_L = 500\ \Omega$; $V_{BAT} = 12$ V; transition from dominant to recessive; note 5; (see Fig.5)	–	16	27	µs
$\Delta t_{slope(norm)}$	normal slope symmetry	normal slope mode; $C_L = 10$ nF; $R_L = 500\ \Omega$; $V_{BAT} = 12$ V; $t_{f(slope)(dom)} - t_{r(slope)(rec)}$	–5	0	+5	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{f(slope)(norm)(dom)}$	normal slope fall time LIN (100% to 0%)	normal slope mode; C_L = 6.8 nF; R_L = 660 Ω; V_{BAT} = 12 V; transition from recessive to dominant; note 4	–	12	22.5	µs
$t_{r(slope)(norm)(rec)}$	normal slope rise time LIN (0% to 100%)	normal slope mode; C_L = 6.8 nF; R_L = 660 Ω; V_{BAT} = 12 V; transition from dominant to recessive; note 5	–	12	22.5	µs
$\Delta t_{slope(norm)}$	normal slope symmetry	normal slope mode; C_L = 6.8 nF; R_L = 660 Ω; V_{BAT} = 12 V; $t_{f(slope)(dom)} - t_{r(slope)(rec)}$	–4	0	+4	µs
$t_{f(slope)(low)(dom)}$	low slope fall time LIN (100% to 0%)	low slope mode; C_L = 10 nF; R_L = 500 Ω; V_{BAT} = 12 V; note 4	–	30	62	µs
$t_{r(slope)(low)(rec)}$	low slope rise time LIN (0% to 100%)	low slope mode; C_L = 10 nF; R_L = 500 Ω; V_{BAT} = 12 V; note 5	–	30	62	µs
t_{BUS}	dominant time for wake-up via bus	sleep mode	30	70	150	µs
t_{NWAKE}	dominant time for wake-up via pin NWAKE	sleep mode	7	20	50	µs
$t_{gotonorm}$	time period for mode change from sleep or standby mode into normal/low slope mode		2	5	10	µs
$t_{gotosleep}$	time period for mode change from normal/low slope mode into sleep mode		2	5	10	µs
t_{dom}	TXD dominant time out	V_{TXD} = 0 V	6	12	20	ms

Notes

1. All parameters are guaranteed over the virtual junction temperature by design, but only 100% tested at 125 °C ambient temperature for dies on wafer level and above this for cased products 100% tested at 25 °C ambient temperature, unless otherwise specified.
2. For bare die, all parameters are only guaranteed if the backside of the bare die is connected to ground.
3. If V_{BAT} is higher than 12 V, the battery current increases due to the internal LIN termination resistor. The minimum value of this resistor is 20 kΩ. The maximum current increase is therefore: $I_{BAT(increase)} = \frac{V_{BAT} - 12\ V}{20\ k\Omega}$
4. $t_{f(slope)(dom)} = \frac{((t_{VLIN} = 40\%) - (t_{VLIN} = 95\%))}{0.55}$; see Fig.6
5. $t_{r(slope)(rec)} = \frac{((t_{VLIN} = 60\%) - (t_{VLIN} = 5\%))}{0.55}$; see Fig.6

TIMING DIAGRAMS

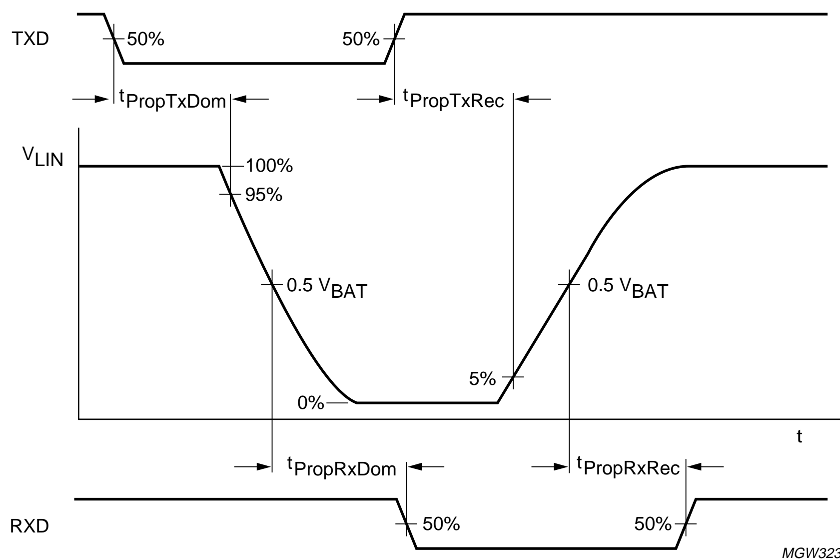


Fig.5 Timing diagram for AC characteristics, bus loaded.

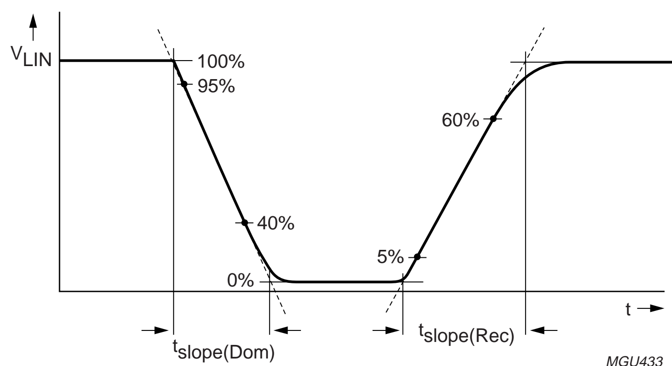
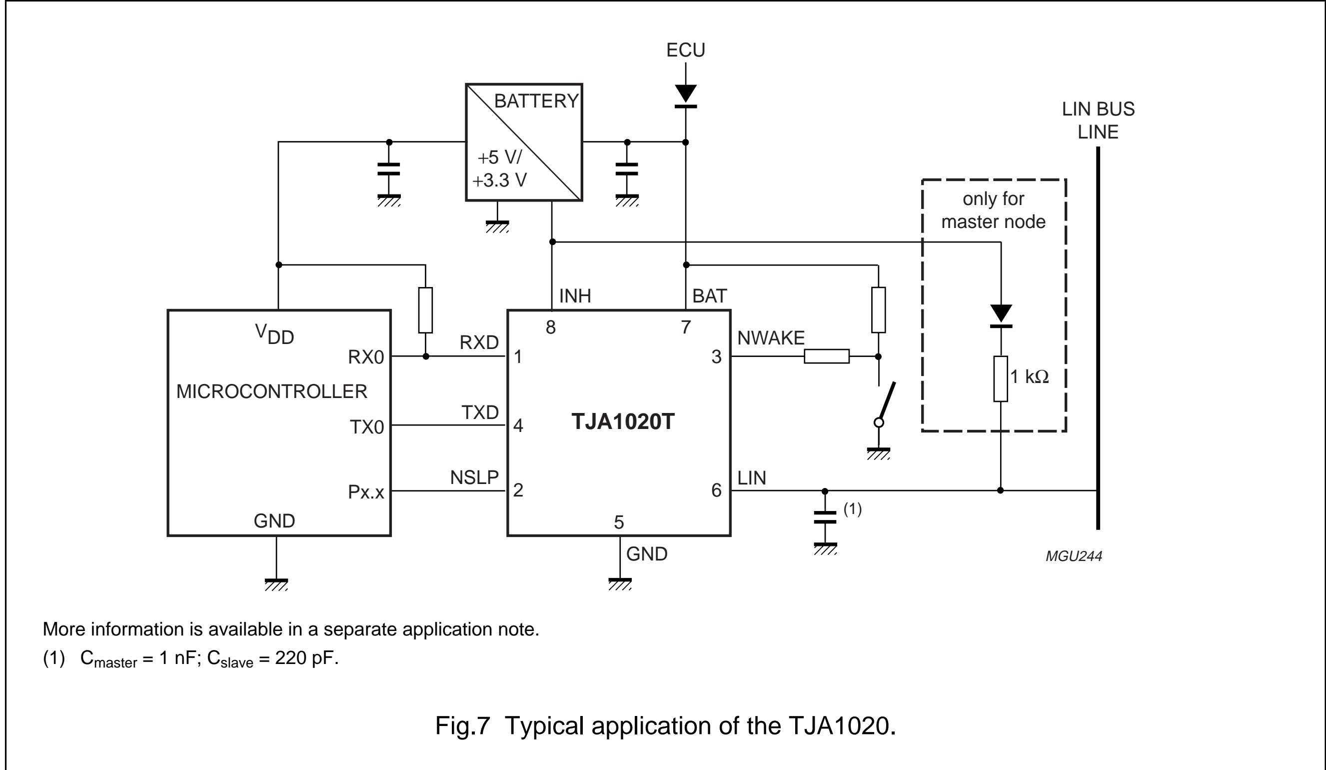


Fig.6 Definition of slope timing.

APPLICATION INFORMATION



More information is available in a separate application note.

(1) C_{master} = 1 nF; C_{slave} = 220 pF.

Fig.7 Typical application of the TJA1020.

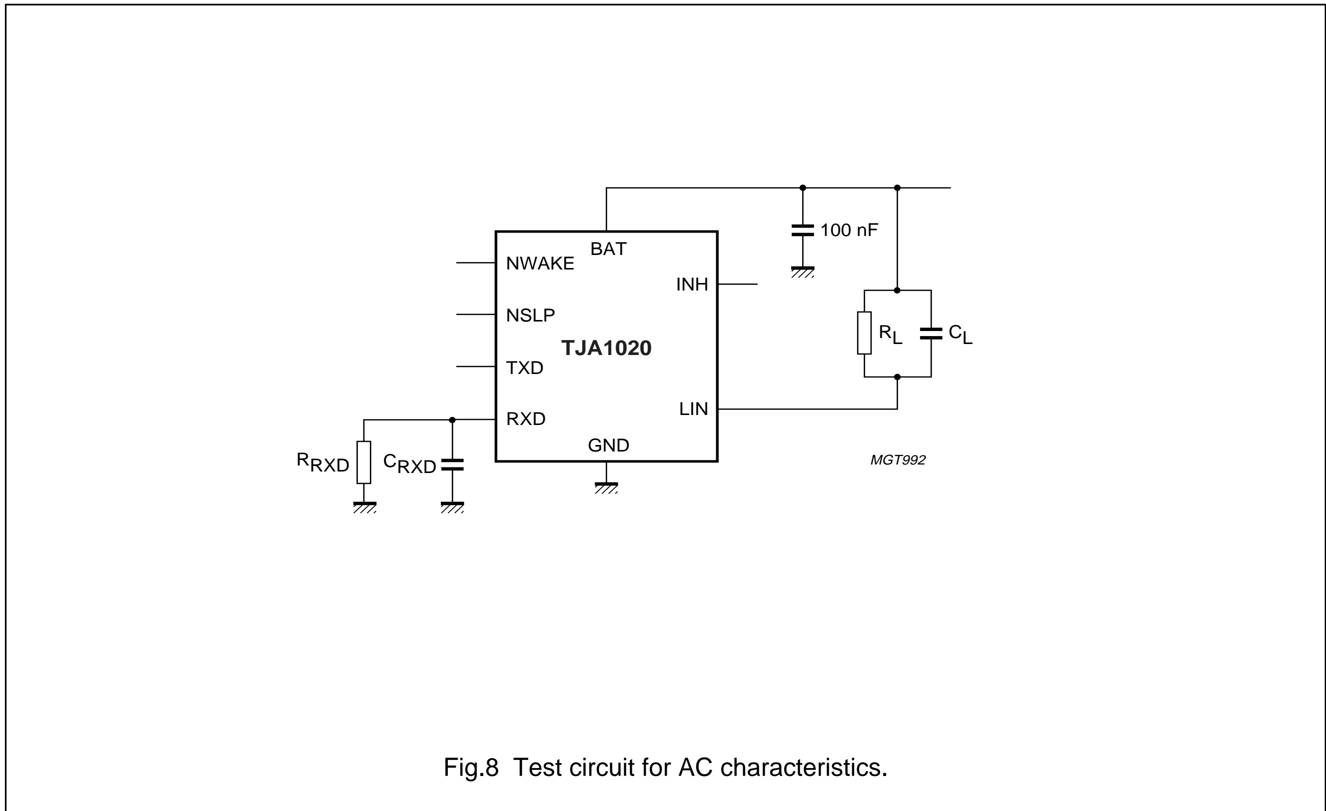
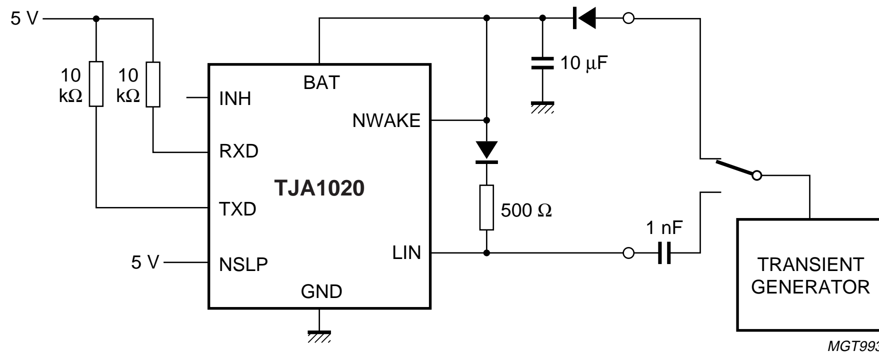


Fig.8 Test circuit for AC characteristics.



The waveforms of the applied transients on pin 6 (LIN) and pin 7 (BAT) are according to ISO7637 part 1, test pulses 1, 2, 3a, 3b, 4, 5, 6 and 7.

Fig.9 Test circuit for automotive transients.

BONDING PAD LOCATIONS

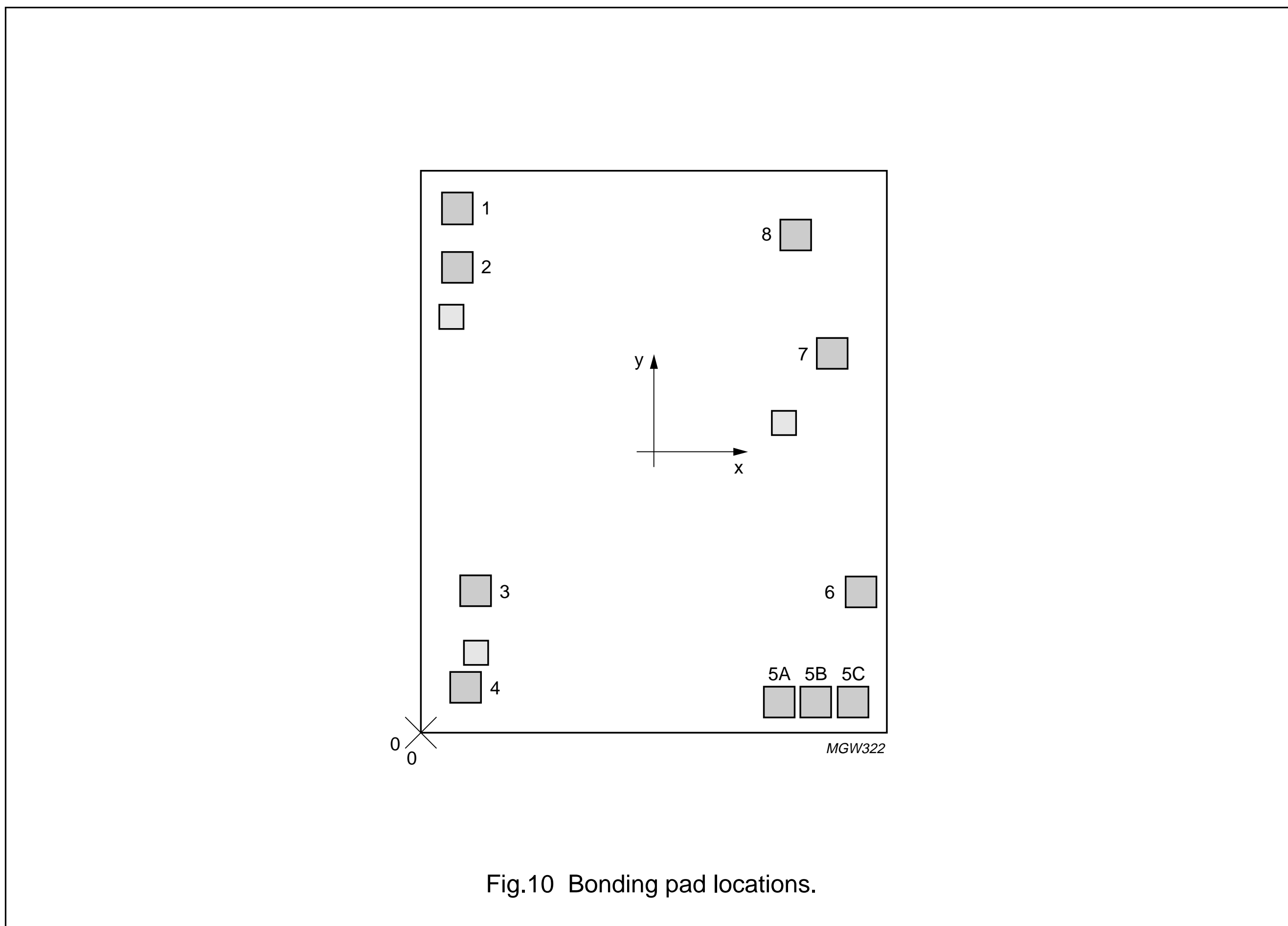


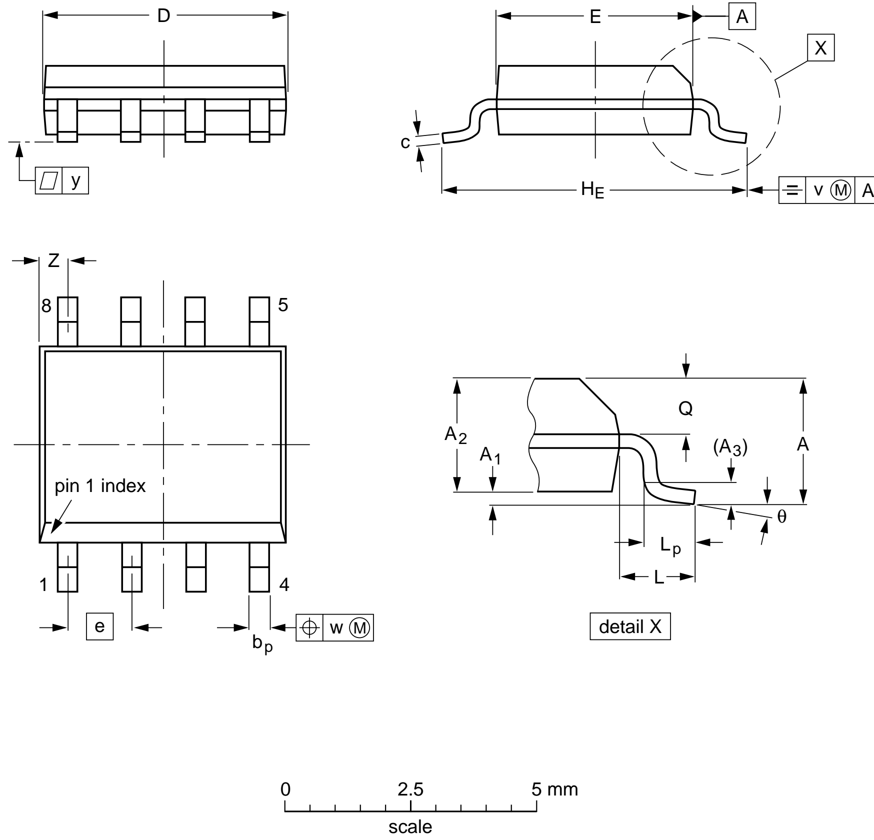
Fig.10 Bonding pad locations.

Table 2 Bonding pad locations (dimensions in μm). All x and y co-ordinates are referenced to the bottom left hand corner of the die.

SYMBOL	PAD	CO-ORDINATES	
		x	y
RXD	1	111	1570
NSLP	2	111	1395
NWAKE	3	165	424
TXD	4	134	134
GND1	5A	1075	90
GND2	5B	1185	90
GND3	5C	1295	90
LIN	6	1318	419
BAT	7	1235	1133
INH	8	1125	1490

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



0 2.5 5 mm
scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[(1)]	SOLDERING METHOD	
	WAVE	REFLOW[(2)]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[(3)]	suitable
PLCC[(4)], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[(4)(5)]	suitable
SSOP, TSSOP, VSO	not recommended[(6)]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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