Power MOSFET

-60 V, -2.6 A, Single P-Channel SOT-223

Features

- Design for low R_{DS(on)}
- Withstands High Energy in Avalanche and Commutation Modes
- AEC-Q101 Qualified NVF2955, NVF2955P
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parame	Symbol	Value	Unit		
Drain-to-Source Voltage			V _{DSS}	-60	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain	Steady T _A = 25°C		I _D	-2.6	Α
Current (Note 1)	State	T _A = 85°C		-2.0	
Power Dissipation (Note 1)	Steady T _A = 25°C		P _D	2.3	W
Continuous Drain	Steady T _A = 25°C		I _D	-1.7	Α
Current (Note 2)	State	T _A = 85°C		-1.3	
Power Dissipation (Note 2)	T _A = 25°C		P _D	1.0	W
Pulsed Drain Current	rain Current tp = 10 μs			-17	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 25 V, V _G = 10 V, I _{PK} = 6.7 A, L = 10 mH, R _G = 25 Ω)			EAS	225	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			TL	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Tab (Drain) - Steady State (Note 2)	$R_{\theta JC}$	14	
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	65	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta,JA}$	150	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.127 in² [1 oz] including traces)
- 2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu. area = 0.341 in²)

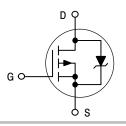


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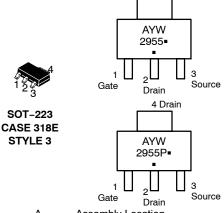
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
-60 V	145 mΩ @ –10 V	-2.6 A

P-Channel



MARKING DIAGRAMS AND PIN ASSIGNMENT

4 Drain



= Assembly Location

= Year

= Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTF2955T1G	SOT-223 (Pb-Free)	1000 /Tape & Reel
NVF2955T1G	SOT-223 (Pb-Free)	1000/ Tape & Reel
NVF2955PT1G	SOT-223 (Pb-Free)	1000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				66.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			-1.0	μΑ
		$V_{DS} = -60 \text{ V}$	T _J = 125°C			-50	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, \	V _{GS} = ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$	I _D = -1.0 mA	-2.0		-4.0	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V	$V_{GS} = -10 \text{ V}, I_D = -0.75 \text{ A}$		145	170	mΩ
		V _{GS} = -10 \	/, I _D = -1.5 A		150	180	
		V _{GS} = -10 \	V _{GS} = -10 V, I _D = -2.4 A		154	185	
Forward Transconductance	9 _{FS}	$V_{GS} = -15 \text{ V}, I_D = -0.75 \text{ A}$			1.77		S
CHARGES AND CAPACITANCES							
Input Capacitance	C _{ISS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 25 \text{ V}$			492		pF
Output Capacitance	C _{OSS}				165		
Reverse Transfer Capacitance	C _{RSS}				50		
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 10 \text{ V}, V_{DS} = 30 \text{ V},$ $I_{D} = 1.5 \text{ A}$			14.3		nC
Threshold Gate Charge	Q _{G(TH)}				1.2		
Gate-to-Source Charge	Q _{GS}				2.3		
Gate-to-Drain Charge	Q_{GD}				5.2		
SWITCHING CHARACTERISTICS (Note	4)			_			
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V,	V _{DD} = 25 V,		11		ns
Rise Time	t _r	$I_D = 1.5 \text{ A}, R_G = 9.1 \Omega$ $R_L = 25 \Omega$			7.6		
Turn-Off Delay Time	t _{d(OFF)}				65		
Fall Time	t _f				38		
DRAIN-SOURCE DIODE CHARACTERIS	STICS					•	
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.5 A	T _J = 25°C		-1.10	-1.30	V
			T _J = 125°C		-0.9		1
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 1.5 \text{ A}$			36		
Charge Time	ta				20		ns
Discharge Time	t _b				16		
Reverse Recovery Charge	Q _{RR}				0.139		nC

Reverse Recovery Charge Q_{RR}
 Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

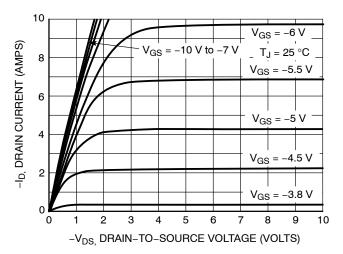


Figure 1. On-Region Characteristics

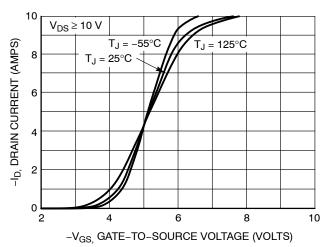


Figure 2. Transfer Characteristics

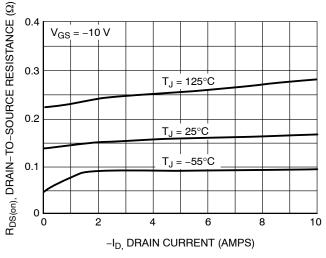


Figure 3. On-Resistance versus Drain Current and Temperature

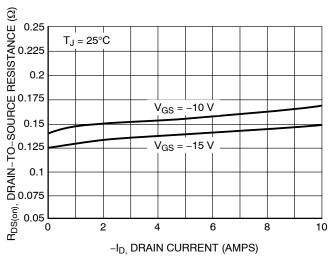
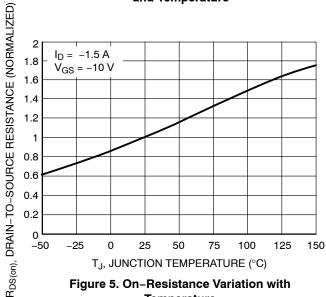


Figure 4. On-Resistance versus Drain Current and Gate Voltage



Temperature

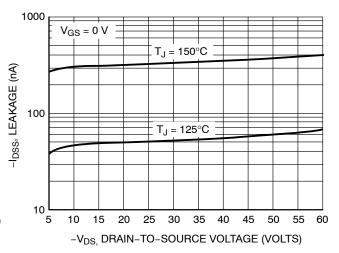
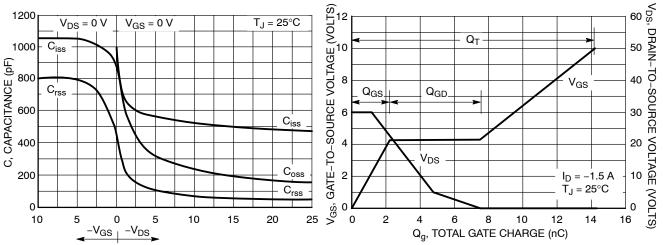


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES (T_{.J} = 25°C unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

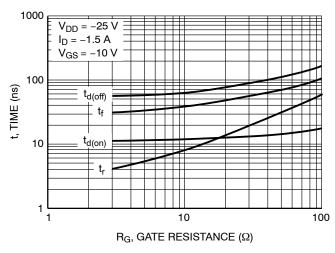


Figure 9. Resistive Switching Time Variation versus Gate Resistance

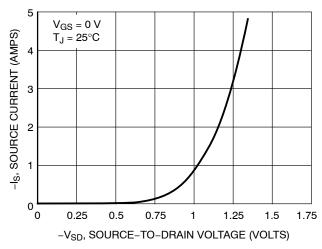


Figure 10. Diode Forward Voltage versus Current

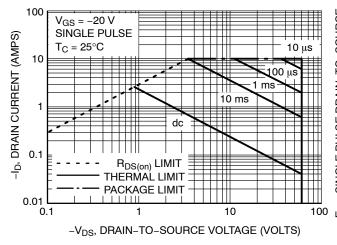


Figure 11. Maximum Rated Forward Biased Safe Operating Area

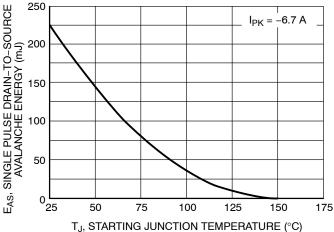
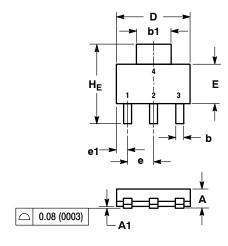
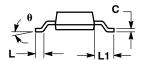


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

PACKAGE DIMENSIONS

SOT-223 (TO-261) CASE 318E-04 ISSUE N



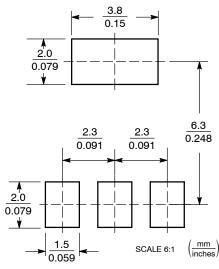


- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
С	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
е	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20			0.008		
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	-	10°	0°	-	10°

- PIN 1. GATE 2. DRAIN
 - SOURCE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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