Independent Review of QT-040398 PCB Pre-production Report

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1 DOCUMENT HISTORY

Issue	Date	Changes / Comments
0.0	05-May-2012	Initial release.

2 INTRODUCTION

Accelerating development from prototype to volume production is one of the keys to profitability for electronic products. Decisions made in the PCB design stage directly affect the success of the New Product Introduction (NPI) process. Any problems found in the PCB design stage generally reduces the number of iterations of hardware and software during NPI process, and often reduces unit manufacturing costs too.

This independent report was created to review the PCB design data from the production point of view, aiming to bridge the gap between PCB design and the mass production engineering. In the context of this report, the following aspects were analyzed. Comments and suggestions were listed in each section.

- Schematic drawing
- Part placement and footprint
- PCB trace routing
- High speed traces and signal integrity
- Silk screen
- Design for Manufacture (DFM)
- Design for Assembly (DFA)
- Design for Test (DFT)
- BOM analysis
- Thermal Analysis
- EMC and ESD
- Power Integrity

3 SCHEMATIC CAPTURE

3.1 It is recommended to input the job name, reversion number in the schematic drawing.

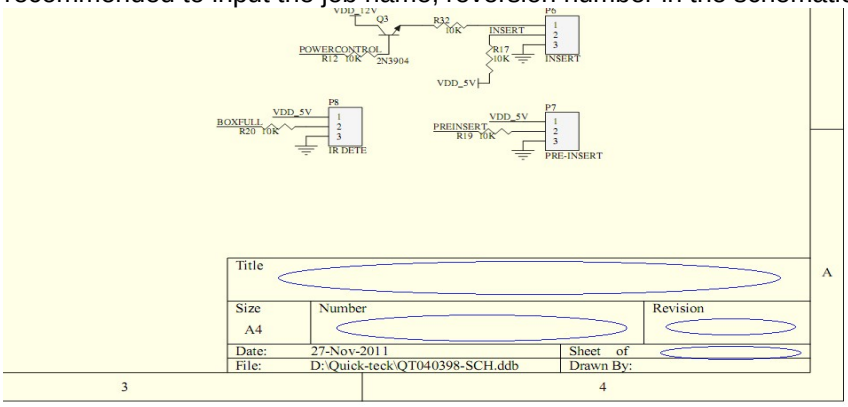
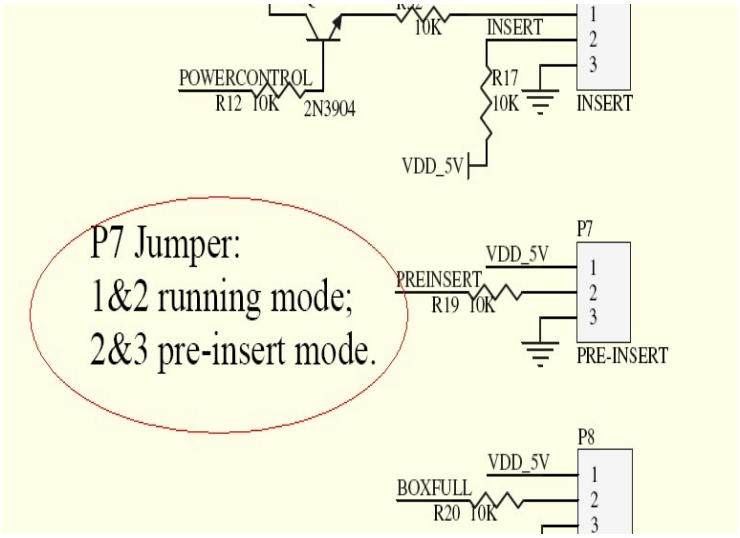


Figure 1 Job information in schemati drawing

3.2 It is recommended to put the Jumper configure instruction in the schematic drawing near the jumper.



3.3 It is suggested to re-organize the schematic diagram with appropriate functional groups. Get the parts which in the same group are close by.

4 TRACE ROUTING

4.1 It is suggested to use 20 to 28 mils Via for these traces connect to power/ground plane. The current design shows the diameter of these vias are only 15 mils . Large vias connected to the power/ground plane leads to better power supply performance.

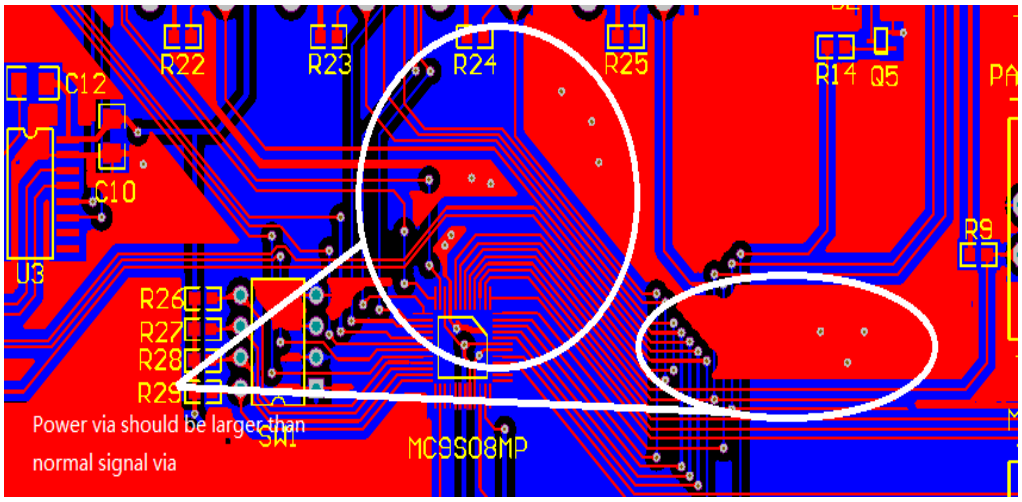
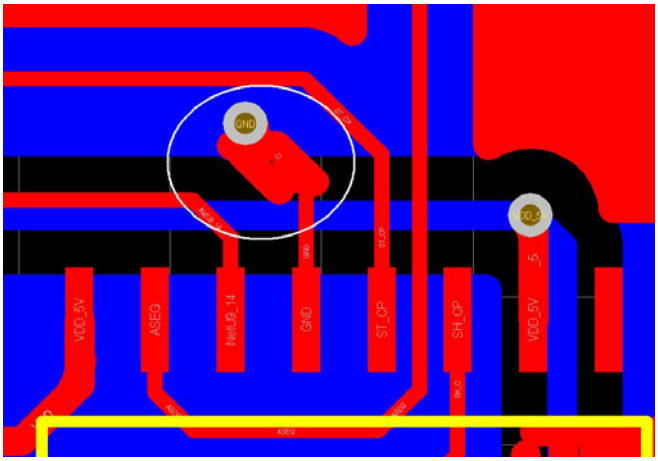


Figure 1 Power via should be larger

4.2 There are few of short traces overlapped each other shown in the following figure. Please use the single trace.



4.3 In the following figure, the trace (net name: TXD) doesn't well connect with the pad. This can be very easily broken during the manufacturing process. Place get the trace fully connected with the pad.

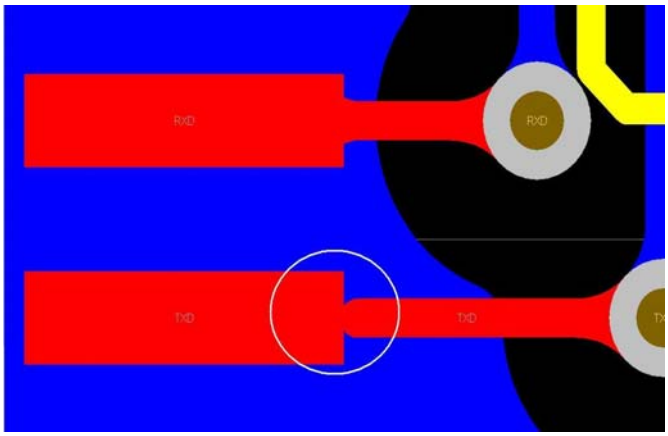
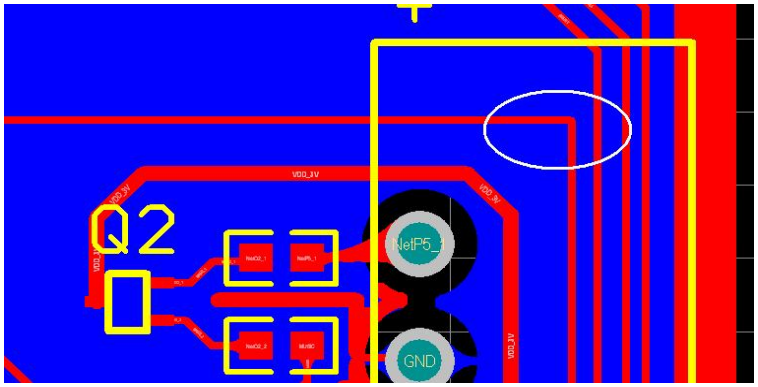


Figure 2 Partly connected trace

4.4 Please use two of 45 degree bend instead of 90 degree at this direction changing point. Two of 45 degree bends are always better from DFM and signal integrity point of view.



4.5 Many pads/vias are defined as teardrop type, while others are standard type. Please see below figure for details.

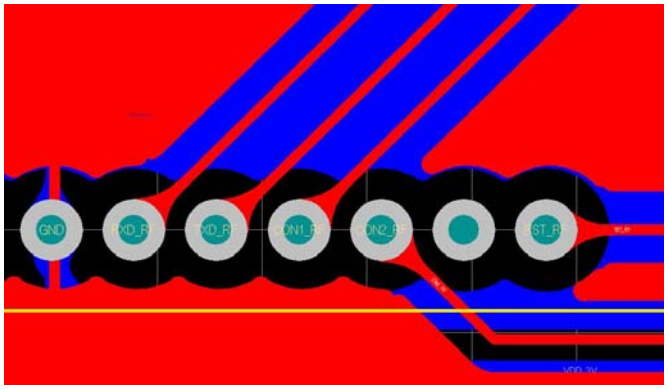


Figure 3 Teardrops

We did not see any special reasons why doing this. Teardrops are normally used to avoid drill breakout where the trace joins the pads/vias. Teardrops can increase the strengthening of the connections between pads/vias and tracks. However, as a professional PCB manufacturer, we only see few scenarios where teardrop could make difference.

1. Single side PCBs, where the holes are non-plated holes (NPTH).
2. HDI PCBs, where the pads/vias diameter are less than 10 mils. This is very often happens near BGA pins or on buried/blind vias on HDI boards.
3. Pads on these components which human interface force maybe involved (e.g. power jack, pin header).
4. Pads on these components which maybe need de-soldering later. Teardrops can help reduce thermal stress on the pads.

None of above situations applies for this design. So we suggest to modify all pads/vias to be standard type.

4.6 The trace shown on below figure doesn't connect to anything after crossing the via (net name: START). It's suggested to delete these extra trace on the board.

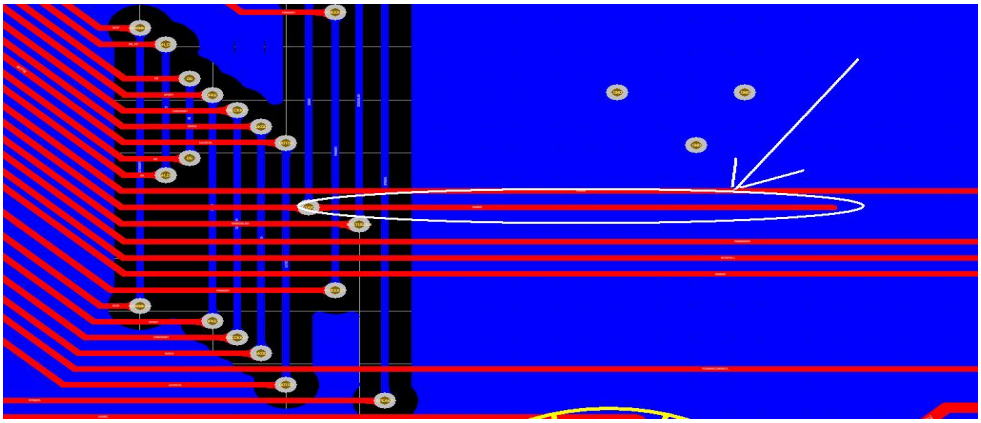


Figure 4 Single end track

4.7 It is recommended to rotate 90 degree of R8 to get better track routing. See below figures for details.

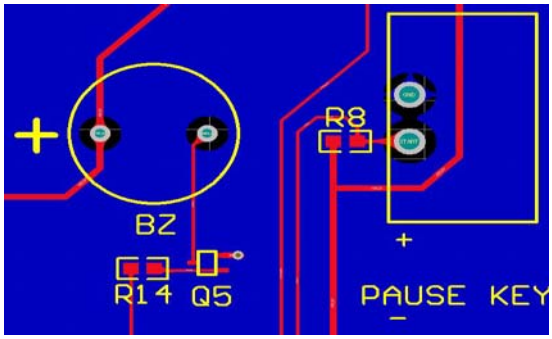


Figure 5 R8 routing (current design)

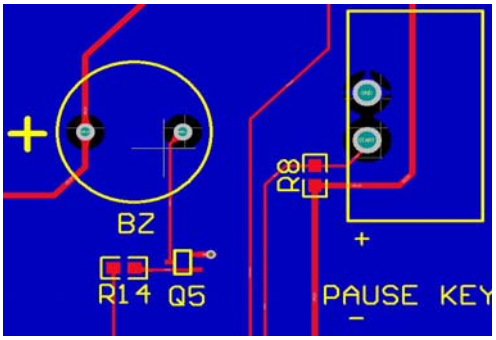


Figure 6 R8 recommended routing

4.8 Rules for high speed traces did not check in this job, as this is not a high speed circuit design (the highest signal speed is 32.768MHz in this design).

5 SILKSCREEN

5.1 'C10' and 'Q4' are overlapped with the vias. The lines on the vias will be removed automatically in the manufacture process. To keep the designator information complete, please move them to a clear area.

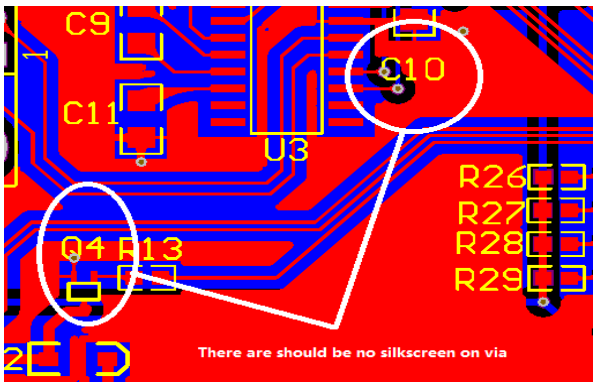


Figure 2 Silkscreen should be not over via

5.2 It's suggested to show the configure information for these switches, jumpers and LEDs on silkscreen layer.

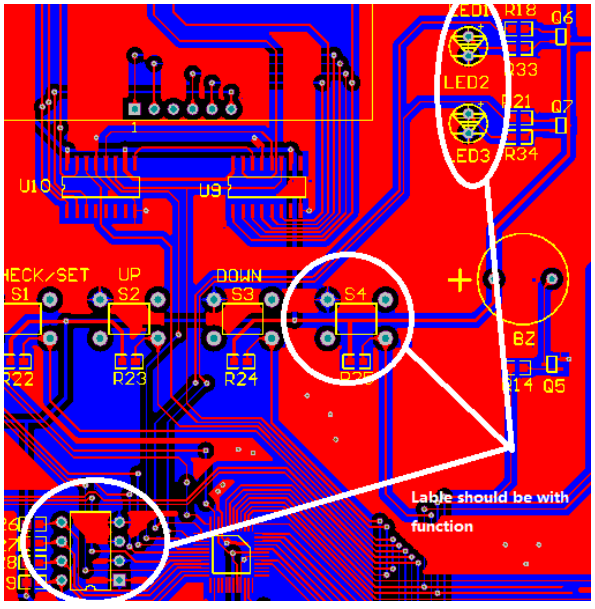


Figure 3 Label should be with function

5.3 ‘J2’ will not be seen when component is installed. Please move them to a visible place.

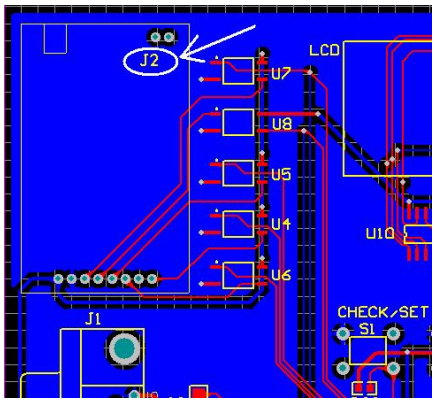


Figure 7 Designator text under the component

5.4 Please use the standard mark(a small ‘+’ or bar on positive side) to show the polarity information for D2.

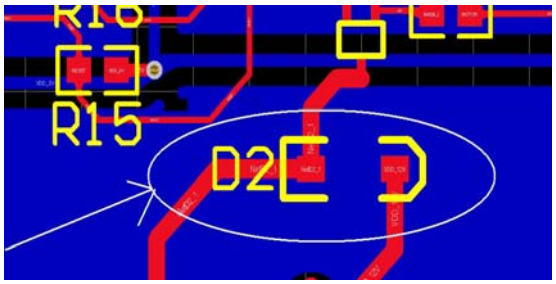


Figure 8 Standard ploarity indication for D2

5.5 There is no pin 1 indication for MC9SO8MP. The pentagon mark cannot be seen when component populated.

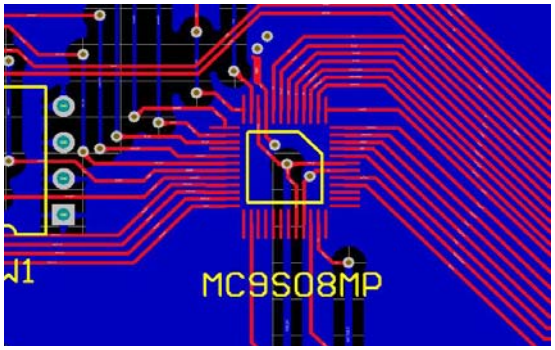


Figure 9 Pin1 indication missing on MPU

5.6 It is recommended to add PCB board information on silkscreen layer (e.g. name, version, date).

6 PART PLACEMENT AND FOOTPRINT

6.1 Having checked with Quick-teck component placement rules, no issues found.

6.2 Having checked with Quick-teck component spacing restrictions, no issues found.

6.3 It is recommended to use IPC-7351 standard footprint for Q1-Q7 (SOT23-3 package).

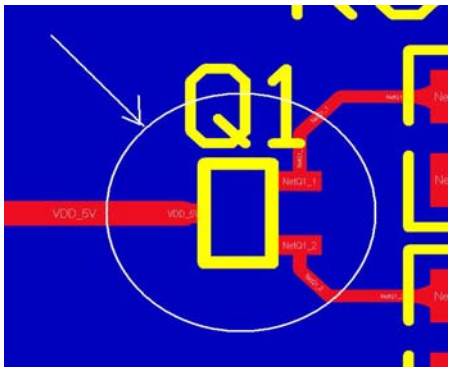


Figure 10 SOT23-3 pad layout (current design)

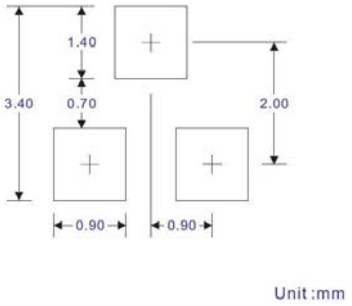


Figure 11 SOT23-3 pad layout (recommended design)

6.4 The current pad width of SOIC-16 is 0.58mm. It is suggested to extend 0.01mm on both side of the pad. So the width pad will be 0.60mm.

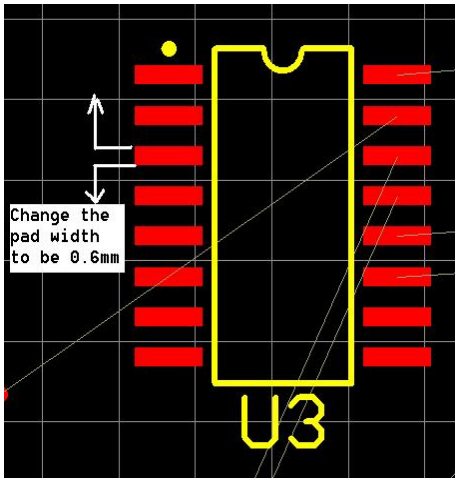


Figure 12 Extend 0.01mm on both side of of the pad

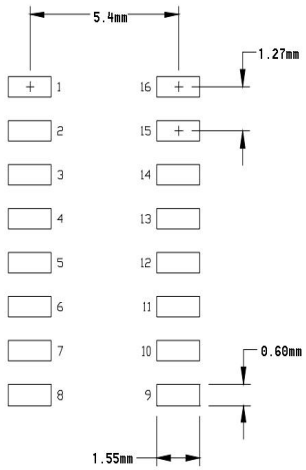


Figure 13 Recommened SOIC-16 pad layout

7 HIGH SPEED TRACES AND SIGNAL INTEGRITY

7.1 There is no transmission line on this design and the highest signal speed is only 32.768MHz), high speed trace rules and signal integrity analysis did not perform on this job.

8 DESIGN FOR MANUFACTURE

8.1 It is recommended to chose the same width value for the traces connected with R22,R23,R24, and R25. From the manufacture point of view, it is always better to use the same width traces connect to one part.

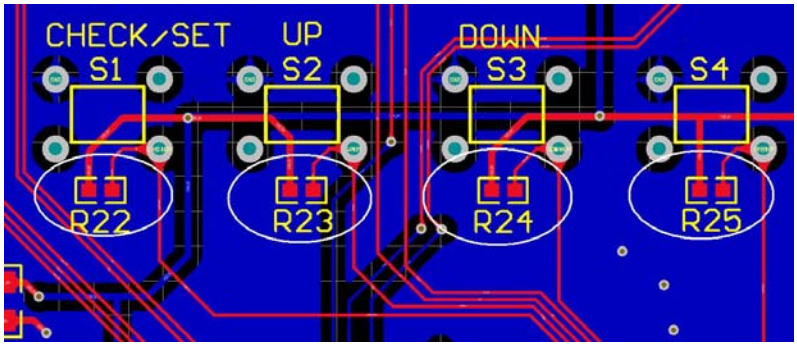


Figure 14 Use the same width trace connect to the part

8.2 It is suggested to extend the trace to the via from the short edge of the pad. If possible, avoid to use 90 degree bend on the trace routing. This is always right from the manufacture point of view.

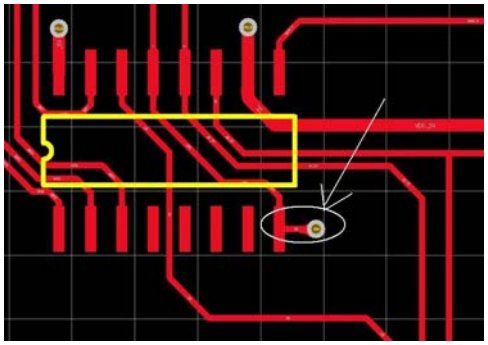


Figure 15 Extended via from long edge (current design)

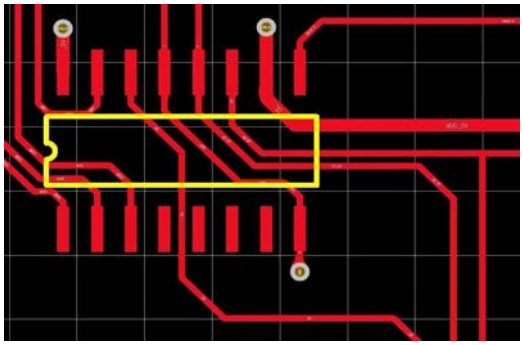


Figure 16 Extended via from short edge (recoomended design)

9 DESIGN FOR ASSEMBLY

9.1 It is recommended to keep these vias at least 15mils away from the IC pads.

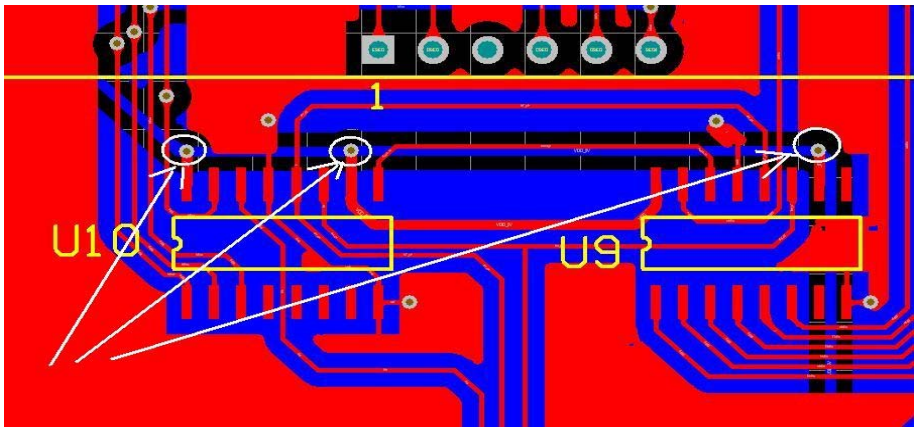


Figure 5 Via should not be so near to pad

9.2 There is a 10mils size via in the central of one of C7 pads. It is suggested to delete it from the pad. The flux could sink into this hole during the reflow soldering process. Practical experience shows drilling hole on the pad could be the root reason of the fake welding.

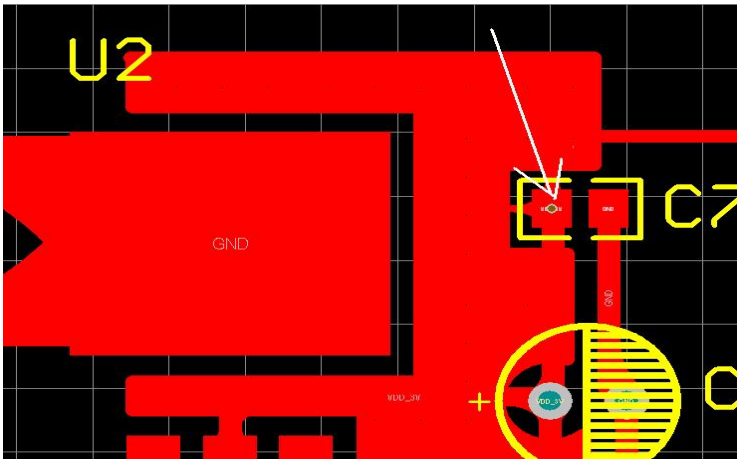


Figure 17 Drill hoel on the pad

9.3 It's recommended to add three of 0.8mm fiducial marks near the corner of the board. This is essential for assembly job done by automated machine.

10 DESIGN FOR TEST

10.1 All tracks have at least one exposed via or pad. Fitting for the test fixture have been considered in this design. No issue found in this section.

11 ALTERNATIVE PART ANALYSIS

11.1 Give the fact that the mass product will be assembled in Far East, it is suggested to use Yageo,Ralec or Samsung 0603 SMT resistors to replace MULTICOMP ones. Yageo,Ralec and Samsung normally have better prices and lead time conditions in Far East. Quick-teck have enough experiences that these two brand parts are compatible with MULTICOMP ones.

Ref	Current part	Recommended part
R1-R7,R10-R34	MULTICOMP: MC 0.063W 0603 1% 10K	Yageo part number: RC0603FR-07010KL
R8,R9	MULTICOMP: MC 0.063W 0603 1% 100K	Yageo part number: RC0603FR-07100KL

12 THERMAL ANALYSIS

12.1 It is suggested to change the diameter of these holes to be 10 mils and add another four holes to get the same thermal dissipation level. Ensure these holes are evenly placed on this big pad. The holes on the current design are 15 mils' big.

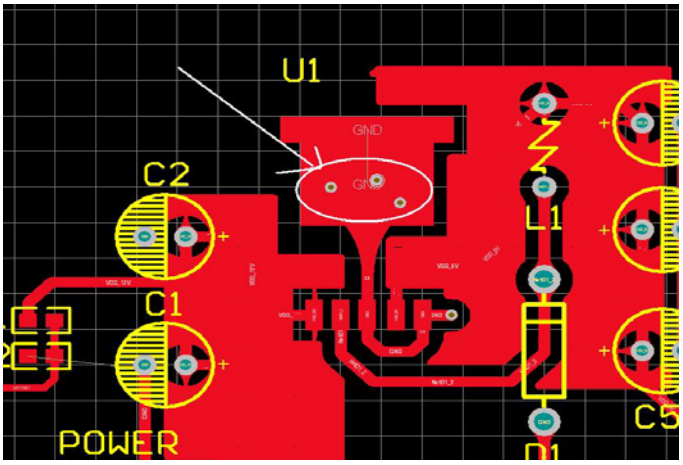


Figure 18 Thermal dissipation holes on voltage regulator

13 EMC AND ESD

13.1 Please place a 25V circuit protection part (TVS diode) at the input side (12V input) of LM2575.

13.2 It is suggested to connect these isolated shapes with ground by Vias.

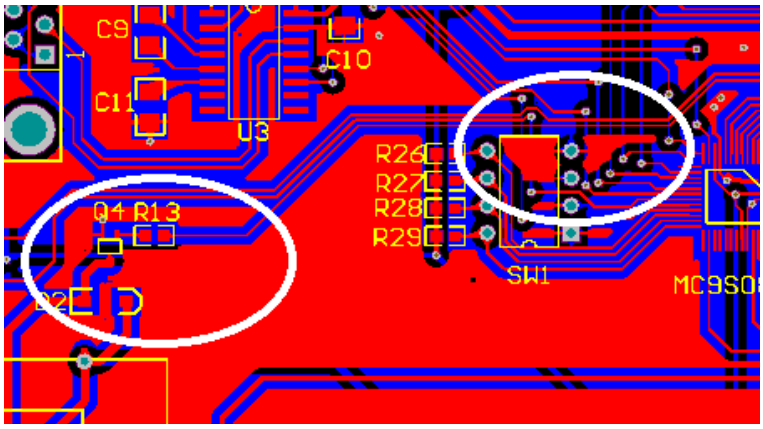


Figure 6 Should not isolated shape plane

14 POWER INTEGRITY

14.1 LM2575 switch regulator are used to create 5V from 12V. To keep the ripple voltage low, its critical to keep the inductor, diode and the switch as close as possible. For the current design, it is suggested to move L1 and D1 150 mils to the left (near to U1).

Figure 19 Keep inductor and diode close to the control device

14.2 It is suggested to use a straight trace for ‘NetD1_2’. This is a switch control signal, So it should be as short as possible (keep the control loop short).

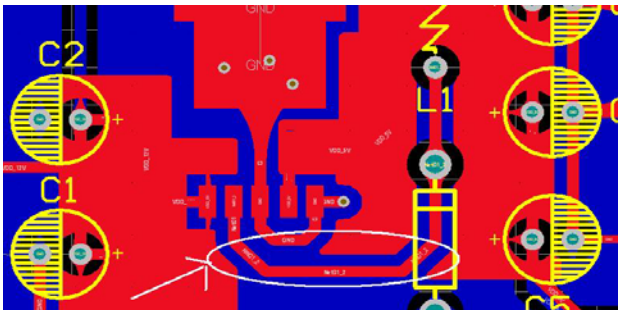


Figure 20 Keep control loop as close as possible

15 PCB DESIGN CHECK LIST RECORD

The samples used in this qualification tests were from the production batch with Ellington PCBs Appendix

Catalog	No.	Details	Record/Notes
Routing	1	All traces have been routed.	Pass
	2	No exposed traces or via under metal cased or similar poorly insulated parts. Better to make these area clear (as keep-out area).	Pass
	3	Use large diameter via for these traces connect to power/ground plane.	Issue 4.1
	4	Check 3W rule for these differential, high speed data or other sensitive signals.	N/A
	5	The minimum width of the traces connected to IC power/ground pins are 6mil (recommend width is 8mil). Keep these trace as short as possible. i.e., connect IC power/ground pins to the power/ground plane through via where nearest possible.	Pass
	6	Use mitered 45 degree bend instead of 90 degree bend where trace changes direction.	Issue 4.4
	7	No traces under crystal/oscillator, transformer, optical coupler, and power supply model.	Pass
Silk Screen	8	All parts should have reference designator values. Designator text should be visible when components are installed.	Pass
	9	Mark pin1 on connectors, pin headers, ICs, crystals, and any other components where pin1 is not readily identifiable.	Issue 5.5
	10	No silkscreen text over vias (if vias not solder masked), pads or holes.	Issue 5.1

	11	The polarity of these polarized component (e.g., cap, diode, LED) should be indicated. This should be visible when component is installed.	Issue 5.4
	12	Switches, jumpers or LEDs are labeled with their functions.	Issue 5.2
	13	All designator texts read in one or two directions (left to right, or top to bottom).	Pass
	14	PCB information shown on silkscreen layer (name, version, data, logo,etc.)	Issue 5.6
Part placement /foot print	15	All components should be placed with an appropriate functional group.	Pass
	16	Print 1:1 scale PCB file, check the footprint by placing the component on it.	Pass
	17	These components which need to be at the fixed position (could be connector, display, switch, button, etc.) have been placed properly.	Pass
	18	Component spacing restriction has been checked	Pass
	19	No parts in keep-out area.	Pass
	20	Heavy components (e.g., coils, transformers) placed near PCB holder or the edge.	Pass
	21	I/O drivers should near where their signals leave the board.	Pass
	22	Board to board connectors (or pin headers) placed near to the edge of PCB.	N/A
High speed trace /signal integrity	23	Series-matching/damping resistors should be close to source side. Termination resistors should be close to target pins.	N/A
	24	One single trace should not change characteristic impedance value over its length.	N/A

	25	These traces, which end to end length are longer than 1/6 of the rising time, is recommended to do signal integration simulation (with simulation tool).	N/A
	26	Bypass capacitors placed close to IC power pins. Each pin have one local bypass cap.	Pass
	27	Digital and analog parts are placed separately. Digital parts on digital ground (DGND) and analog parts on analog ground (AGND). Put a ferrite bead between analog and digital ground to reduce interference.	N/A
	28	Keep clock traces as straight and short as possible. Minimize the number of via in clock transmission lines.	Pass
	29	High speed singles design rule check (termination, impedance, reference plane, EMI, multi-points connection to apology, etc.).	N/A
	30	Run the differential traces as closely as possible after they leave the source parts.	N/A
	31	Minimize the number of via over these high speed differential traces.	N/A
	32	The lengths between the differential traces should be the same.	N/A
	33	PCB layer stickup (multilayer PCB) has been properly setup in achieving the best possible electrical performance.	N/A
Design for Manufacture	34	Perform DRC check to ensure the design meets manufacturing capabilities	Pass
	35	On power/ground plane, distribute via density about the available space as evenly as possible.	Pass

	36	On one single trace, in the case the trace width need to be changed (this normally happens on the traces from small chips, BGAs or fine pitch component pins), the increased/decreased width at one place should not larger than the thinnest trace width. For example, if the traces need change from 8mil to 24mil, use a piece of 16mil trace as transition wire.	Pass
	37	No Trace/via/pad within 20mil around non-plating holes at inner layers. This value changes to 12mil for outer layers.	Pass
	38	For these chip components (0805 and smaller package), ensure the trace width is the same on both side of it.	Issue 8.1
	39	Keep at least 8mil between adjacent copper pours.	Pass
Design for Assembly	40	Three global fiducially marks should be located on PCB that contain components to be mounted with automated machine.	Issue 9.3
	41	All Fine Pitch or BGA package footprints need two local fiducially marks if automated machine used for fitting them.	N/A
	42	The global fiducially marks should be located at the corner area (3.0mm to 5.5mm distance to the edge) or the frame of the panel.	N/A
	43	The recommended size for fiducially mark is 1.0mm.	N/A
	44	Keep clear within 3.0mm around the fiducial marks.	N/A
	45	Finished hole sizes are at least 10mils larger than the fitting leads (Thrum-hole parts).	N/A
	46	For SMT pads, the length are at least 8mil longer than pins' length (4mil each side). The width should be at least equal to pads' width.	N/A

	47	Aligning/mechanical holes are recommended to be non-plated. In the case plating aligning/mechanical holes are used ensure don't expose the pads on soldering side. Otherwise peelable ink should be used in wave soldering process (cost increased).	Pass
	48	No trace/via/pad within 1.5mm around the mechanical holes. This value increases to 3.0mm if the screw/washer are conductive (metal material) one.	Pass
	49	Better to have reference designator value for each mechanical hole. This information is helpful in assembly process.	N/A
	50	All via/hole under BGA should be filled and covered by solder mask. PCB manufacturers normal do this by default.	N/A
	51	No via/hole on the pads of these components populated with reflow machine. Keep solder-masked via/hole at least 15mil away from the pads. This value increase to 20mil, if the via/hole are exposed one.	Issue 9.2
	52	On component side, no parts within 3.0mm area to plug sockets (or pin headers). No components and pads under these sockets (or pin headers) on the soldering side.	Pass
	53	Thermal relief pad used for these pads which could have cold soldered joint issue (e.g., power/ground pins of through-hole parts).	Pass
Design for Test	54	Test pads/via have added on these important signals. These pads/vias should not be placed within 5mm of the edge.	Pass
	55	Test vias are exposed.	Pass
	56	No logic pins connected directly to power/ground if in-circuit test is planned.	N/A
	57	JTAG header included on board (connected to JTAG pins of devices)	N/A

		where possible.	
Thermal Analysis	58	Thermal considerations require that the component density be distributed about the available board space as evenly as possible.	Pass
	59	For these high power dissipation parts (e.g., FET, LDO, DC/DC module), make enough copper coverage on all the layers. Also thermal via (plated thrum-holes) are needed under the package.	Pass
	60	Locate these temperature-sensitive components (e.g., electrolytic cap, oscillator) away from hot part (e.g., transformer, heat sink).	Pass
	61	Thermal land (exposed copper area directly underneath the body of the hot component. e.g., LDO) should not covered by solder mask.	Pass
EMC and ESD	62	Crystal case should be flush to the PCB and grounded.	N/A
	63	These circuit protection parts (e.g., PTC thermostat, TVS diode) close to the parts/sockets being protected.	Issue 13.1
	64	For multilayer PCBs, check 20H rule for power and ground plane.	N/A
	65	No isolated shapes on power/ground plane.	Issue 13.2
	66	Hatched copper pour (12mil trace and 20mil pitch) rather than solid copper pour where possible.	N/A
	67	Avoid small copper area and sharp shape area as this may act as antennae and emit noise.	Pass
Power Integrity	68	Minimizing the current loop in power supply design. If the board power is supplied by switch mode, the switching parts (e.g., FET, inductor, diode, and capacitor) should be as close as possible.	Issue 14.1
	69	Check the current capability. A practical rule: 1oz copper weight: 1A/mm width.	Pass

16 NOTE

Quick-teck assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications with Quick-teck report as reference. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.